L Number	Hits	Search Text	DB	Time stamp
1	20	"5905998"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:18
2	21936	partition$4 same block	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:21
3	12811	(partition$4 same block) and process$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:28
4	1965	((partition$4 same block) and process$4) and (716/$.ccls. or 703/$.ccls. or 711/$.ccls. or 704/$.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:32
5	1457	(((partition$4 same block) and process$4) and (716/$.ccls. or 703/$.ccls. or 711/$.ccls. or 704/$.ccls.)) and identif$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:32
6	1054	((((partition$4 same block) and process$4) and (716/$.ccls. or 703/$.ccls. or 711/$.ccls. or 704/$.ccls.)) and identif$4) and physical	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:33
7	479	(((((partition$4 same block) and process$4) and (716/$.ccls. or 703/$.ccls. or 711/$.ccls. or 704/$.ccls.)) and identif$4) and physical) and port	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:44
8	1784	identif$4 same physical same port	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 18:33
9	12	(identif$4 same physical same port) and (((partition$4 same block) and process$4) and (716/$.ccls. or 703/$.ccls. or 711/$.ccls. or 704/$.ccls.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:46
10	6515	(partition$4 same block) and (milti-processor or multiprocessor or processor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:48
11	85	((partition$4 same block) and (milti-processor or multiprocessor or processor)) and (identif$4 same physical same port)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 17:48
12	26251	identif$4 same port	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 18:33
13	773	(partition$4 same block) and (identif$4 same port)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 18:53

14	581	((partition$4 same block) and (milti-processor or multiprocessor or processor)) and (identif$4 same port)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 18:54
15	53	(((partition$4 same block) and (milti-processor or multiprocessor or processor)) and (identif$4 same port)) and join	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 18:55
16	173	(((partition$4 same block) and (milti-processor or multiprocessor or processor)) and (identif$4 same port)) and join$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 18:55
17	50	((((partition$4 same block) and (milti-processor or multiprocessor or processor)) and (identif$4 same port)) and join$4) and bind$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/01 18:56

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20030161315 A1	20030828	10	Memory system with apparatus and method to enable balanced bandwidth utilization	370/395.1
2	US 20030131330 A1	20030710	17	Masterless building block binding to partitions	716/7
3	US 20030131214 A1	20030710	36	Masterless building block binding to partitions using identifiers and indicators	712/13
4	US 20030131154 A1	20030710	16	Building block removal from partitions	710/1
5	US 20030131067 A1	20030710	24	Hardware support for partitioning a multiprocessor system to allow distinct operating systems	709/213
6	US 20030093253 A1	20030515	28	Grammar for message passing in a distributed simulation environment	703/13
7	US 20030037127 A1	20030220	33	Silicon-based storage virtualization	709/220
8	US 20020129176 A1	20020912	11	SYSTEM AND METHOD FOR ESTABLISHING DIRECT COMMUNICATION BETWEEN PARALLEL PROGRAMS	709/313
9	US 20020078040 A1	20020620	21	Apparatus and method for providing a binary range tree search	707/4
10	US 20020065963 A1	20020530	16	Method and system for flexible channel path identifier assignment	710/38
11	US 20020061012 A1	20020523	119	Cable modem with voice processing capability	370/352
12	US 20020010735 A1	20020124	70	Multicast transmissions in a multistage interconnect network	709/201
13	US 20020007360 A1	20020117	21	Apparatus and method for classifying information received by a communications system	707/4
14	US 20020006137 A1	20020117	52	System and method for supporting multiple voice channels	370/466

	Document ID	Issue Date	Pages	Title	Current OR
15	US 20010033583 A1	20011025	72	Voice gateway with downstream voice synchronization	370/503
16	US 20010029590 A1	20011011	17	Processor having execution core sections operating at different clock rates	713/501
17	US 6631454 B1	20031007	16	Processor and data cache with data storage unit and tag hit/miss logic operated at a first and second clock frequencies	711/167
18	US 6601190 B1	20030729	22	Automatic capture and reporting of computer configuration data	714/37
19	US 6539435 B2	20030325	11	System and method for establishing direct communication between parallel programs	709/310
20	US 6519595 B1	20030211	20	Admission control, queue management, and shaping/scheduling for flows	707/10
21	US 6487675 B2	20021126	17	Processor having execution core sections operating at different clock rates	713/501
22	US 6446090 B1	20020903	22	Tracker sensing method for regulating synchronization of audit files between primary and secondary hosts	707/201
23	US 6430577 B1	20020806	21	System and method for asynchronously receiving multiple packets of audit data from a source databased host in a resynchronization mode and asynchronously writing the data to a target host	707/201
24	US 6424248 B1	20020723	83	Furniture unit having a modular communication network	340/3.51
25	US 6295532 B1	20010925	21	Apparatus and method for classifying information received by a communications system	707/4

	Document ID	Issue Date	Pages	Title	Current OR
26	US 6278995 B1	20010821	19	Apparatus and method for providing a binary range tree search	707/4
27	US 6256745 B1	20010703	17	Processor having execution core sections operating at different clock rates	713/501
28	US 6243361 B1	20010605	61	Multistage interconnect network uses a master processor to perform dynamic configuration for all switch nodes based on a predetermined topology	370/254
29	US 6216234 B1	20010410	15	Processor having execution core sections operating at different clock rates	713/501
30	US 6211796 B1	20010403	79	Communications network for identifying the location of articles relative to a floor plan	340/825.49
31	US 6133845 A	20001017	82	Furniture unit having a modular communication network	340/310.08
32	US 5966544 A	19991012	17	Data speculatable processor having reply architecture	712/32
33	US 5942984 A	19990824	79	Communications network for identifying the location of articles relative to a floor plan	340/3.5
34	US 5925097 A	19990720	42	Directly programmable distribution element	709/200
35	US 5913164 A	19990615	90	Conversion system used in billing system for mobile satellite system	455/427

	Document ID	Issue Date	Pages	Title	Current OR
36	US 5907285 A	19990525	81	Furniture unit having a modular communication network	340/3.5
37	US 5872904 A	19990216	60	Computer system using a master processor to automatically reconfigure faulty switch node that is detected and reported by diagnostic processor without causing communications interruption	714/4
38	US 5828868 A	19981027	16	Processor having execution core sections operating at different clock rates	713/501
39	US 5802052 A	19980901	45	Scalable high performance switch element for a shared memory packet or ATM cell switch fabric	370/395.72
40	US 5754764 A	19980519	143	Combination of input output circuitry and local area network systems	709/200
41	US 5684469 A	19971104	83	Method of configuring a furniture utility distribution system	340/825.52
42	US 5634004 A	19970527	43	Directly programmable distribution element	710/317
43	US 5530435 A	19960625	78	Utility distribution system for modular furniture and the like	340/825.52
44	US 5522046 A	19960528	62	Communication system uses diagnostic processors and master processor module to identify faults and generate mapping tables to reconfigure communication paths in a multistage interconnect network	709/239

	Document ID	Issue Date	Pages	Title	Current OR
45	US 5450073 A	19950912	20	Controlling power sequencing of a control unit in an input/output system	340/3.1
46	US 5430726 A	19950704	84	Repeater interface controller with a shared data bus	370/438
47	US 5423006 A	19950606	18	Notification and verification of state changes in a data processing input/output system	710/19
48	US 5420998 A	19950530	21	Dual memory disk drive	711/113
49	US 5420988 A	19950530	16	Establishing logical paths through a switch between channels and control units in a computer I/O system	712/300
50	US 5414851 A	19950509	36	Method and means for sharing I/O resources by a plurality of operating systems	709/104
51	US 5396495 A	19950307	70	Hub management bus architecture for repeater interface controller	370/408
52	US 5384767 A	19950124	83	Segment tester for a repeater interface controller	370/408
53	US 5371897 A	19941206	14	Method for requesting identification of a neighbor node in a data processing I/O system	709/222
54	US 5321813 A	19940614	69	Reconfigurable, fault tolerant, multistage interconnect network and protocol	714/798
55	US 5303383 A	19940412	60	Multiprocessor computer system	712/43
56	US 5299195 A	19940329	84	Repeater interface controller with multiple port node interfaces	370/462
57	US 5293375 A	19940308	83	Repeater interface controller with a partitioning port state machine	370/445

	Document ID	Issue Date	Pages	Title	Current OR
58	US 5276813 A	19940104	12	Acquiring addresses in an input/output system	710/9
59	US 5117350 A	19920526	34	Memory address mechanism in a distributed memory architecture	711/1
60	US 5107489 A	19920421	18	Switch and its protocol for making dynamic connections	370/360
61	US 5081675 A	19920114	36	System for protection of software in memory against unauthorized use	713/190
62	US 4985825 A	19910115	22	System for delaying processing of memory access exceptions until the execution stage of an instruction pipeline of a virtual memory system based digital computer	711/169
63	US 4977582 A	19901211	62	Synchronization of non-continuous digital bit streams	375/371
64	US 4958341 A	19900918	63	Integrated packetized voice and data switching system	370/352
65	US 4942574 A	19900717	63	Concurrent resource request resolution mechanism	370/400
66	US 4932826 A	19900612	93	Automated cartridge system	414/277
67	US 4928245 A	19900522	89	Automated cartridge system	700/218
68	US 4922486 A	19900501	62	User to network interface protocol for packet communications networks	370/427
69	US 4899333 A	19900206	62	Architecture of the control of a high performance packet switching distribution network	370/427
70	US 4897874 A	19900130	62	Metropolitan area network arrangement for serving virtual data networks	713/201

	Document ID	Issue Date	Pages	Title	Current OR
71	US 4896319 A	19900123	62	Identification and authentication of end user systems for packet communications network services	370/427
72	US 4894824 A	19900116	63	Control network for a rapid connection circuit switch	370/380
73	US 4893302 A	19900109	61	Arrangement for switching concentrated telecommunications packet traffic	370/427
74	US 4875206 A	19891017	61	High bandwidth interleaved buffer memory and control	370/427
75	US 4872160 A	19891003	64	Integrated packetized voice and data switching system	370/353
76	US 4872159 A	19891003	62	Packet network architecture for providing rapid response time	370/352
77	US 4872158 A	19891003	62	Distributed control rapid connection circuit switch	370/380
78	US 4872157 A	19891003	63	Architecture and organization of a high performance metropolitan area telecommunications packet network	370/400
79	US 4864511 A	19890905	103	Automated cartridge system	700/218
80	US 4825438 A	19890425	394	Bus error detection employing parity verification	714/56
81	US 4734909 A	19880329	396	Versatile interconnection bus	370/462
82	US 4625081 A	19861125	146	Automated telephone voice service system	379/88.26
83	NN9707191	19970701	NA	Configurable Cache Memory System	

	Document ID	Issue Date	Pages	Title	Current OR
84	NN9302151	19930201	1	Memory Organization Scheme for the Implementation of Routing Tables in High Performance IP Routers	
85	US 20030131330 A	20030710	17	Master less building block binding method for multiprocessor systems, involves sending physical port identifiers indicating logical location of building block, receiving and joining partition indicated by identifiers	

```
Set     Items   Description
S1        267   AU=(DOWNER W? OR DOWNER, W? OR GILBERT B? OR GILBERT, B? OR
               LOVETT T? OR LOVETT, T? OR SHAH, M? OR SHAH M)
S2    1132522   IC = G06F?
S3      11500   BUILDING(2N)BLOCK?
S4          4   S1 AND S2 AND S3
S5          4   IDPAT (sorted in duplicate/non-duplicate order)
S6          4   IDPAT (primary/non-duplicate records only)
?  show files
File 347:JAPIO Oct 1976-2003/Jun(Updated 031006)
         (c) 2003 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2003/Oct W01
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20031009,UT=20031002
         (c) 2003 WIPO/Univentio
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200365
         (c) 2003  Thomson Derwent
?
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6/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015600231 **Image available**
WPI Acc No: 2003-662386/200362
XRPX Acc No: N03-528650
Master less building block **binding method for multiprocessor systems, involves sending physical port identifiers indicating logical location of** building block **, receiving and joining partition indicated by identifiers**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: **DOWNER W A ; GILBERT B M ; LOVETT T D** ; SHAH M M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030131330	A1	20030710	US 200245926	A	20020109	200362	B

Priority Applications (No Type Date): US 200245926 A 20020109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030131330	A1		17	G06F-009/45	

Abstract (Basic): US 20030131330 A1
NOVELTY - The method involves sending a physical port and partition identifier to another **building block** . Then receiving another port and partition identifier from another block. A logical port identifier identified by the former partition identifier is sent to the subset of blocks. Then receiving another logical port identifiers. Finally joining the former partition identifier with the **building block** .
DETAILED DESCRIPTION - The operation of sending and receiving physical port and partition identifiers is also done for a subset of both the **building blocks** in a similar way. An INDEPENDENT CLAIM is also included for a system for binding **building blocks** of multiprocessor systems.
USE - Used for binding **building blocks** in a multiprocessor computer system.
ADVANTAGE - The failure of any one building does not prevent the others from properly binding to their respective partitions. Race conditions are avoided through the use of various identifiers and indicators of the **building blocks** and partitions are also protected from rogue software.
DESCRIPTION OF DRAWING(S) - The drawing shows a flowchart of a method for binding a **building block** of a platform to a partition of the platform.
pp; 17 DwgNo 1/6
Title Terms: MASTER; LESS; BUILD; BLOCK; BIND; METHOD; MULTIPROCESSOR; SYSTEM; SEND; PHYSICAL; PORT; IDENTIFY; INDICATE; LOGIC; LOCATE; BUILD; BLOCK; RECEIVE; JOIN; PARTITION; INDICATE; IDENTIFY
Derwent Class: T01
International Patent Class (Main): **G06F-009/45**
International Patent Class (Additional): **G06F-017/50**
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05E

6/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015600182 **Image available**
WPI Acc No: 2003-662337/200362
XRPX Acc No: N03-528601
Masterless building block **partitioning method for multi-processor computer systems, involves communicating** building blocks **to determine uniqueness of block partition and joining unique partition by each** building blocks
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: **DOWNER W A ; GILBERT B M ; LOVETT T D**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030131214	A1	20030710	US 200245796	A	20020109	200362	B

Priority Applications (No Type Date): US 200245796 A 20020109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030131214	A1		36	G06F-015/00	

Abstract (Basic): US 20030131214 A1
NOVELTY - The method involves communicating among many **building blocks** to send a partition identifier that determines a partition for each of the **blocks** . The **building blocks** are communicated to determine the uniqueness of the partition. The unique partition is joined by each of the **building blocks** .
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) a masterless **building block** partitioning system
(b) an article having a computer readable medium for a method of partitioning masterless **building block** .
USE - Used for partitioning masterless **building blocks** of multi-processor computer systems.
ADVANTAGE - The method does not prevent any of the **building blocks** from binding properly on failure of the **building blocks** . The **building blocks** are protected from other **building blocks** , as well as from rogue software. The race conditions are avoided through the use of the partition identifier.
DESCRIPTION OF DRAWING(S) - The drawing shows a flowchart of a method for masterless binding of **building blocks** to partitions.
pp; 36 DwgNo 1/15
Title Terms: BUILD; BLOCK; PARTITION; METHOD; MULTI; PROCESSOR; COMPUTER; SYSTEM; COMMUNICATE; BUILD; BLOCK; DETERMINE; BLOCK; PARTITION; JOIN; UNIQUE; PARTITION; BUILD; BLOCK
Derwent Class: T01
International Patent Class (Main): **G06F-015/00**
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05E; T01-M02; T01-S03

6/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015600143 **Image available**
WPI Acc No: 2003-662298/200362
XRPX Acc No: N03-528562
Platform building block **removing method, involves halting activity by partition of** building block **, withdrawing resources from block and deauthorizing block from partition**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: **DOWNER W A** ; **GILBERT B M** ; **LOVETT T D** ; SHAH M M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030131154	A1	20030710	US 200245774	A	20020109	200362	B

Priority Applications (No Type Date): US 200245774 A 20020109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030131154	A1		16	G06F-003/00	

Abstract (Basic): US 20030131154 A1

NOVELTY - The method involves halting input/output activity by a partition on a **building block** (202a) and an identifier of the block having joined to the partition in a masterless manner indicates the partition. The resources of the block are then withdrawn and deauthorized from the partition. The deauthorization includes turning OFF a commit indicator of the **building block** .

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a system for removing blocks from partition of a platform.

USE - Used for removing blocks from partition.

ADVANTAGE - The masterless join of the block with partition helps in removing the block easily from the partition. The method helps in ensuring the orderly binding of **building blocks** into the partitions.

DESCRIPTION OF DRAWING(S) - The drawing shows a diagram of a platform with **building blocks** having partitions.

Building block . (202a)

pp; 16 DwgNo 2/6

Title Terms: PLATFORM; BUILD; BLOCK; REMOVE; METHOD; HALT; ACTIVE; PARTITION; BUILD; BLOCK; WITHDRAW; RESOURCE; BLOCK; BLOCK; PARTITION
Derwent Class: T01
International Patent Class (Main): **G06F-003/00**
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05E; T01-F05G; T01-S03
?

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Set     Items   Description
S1         97   MASTERLESS OR MASTER()LESS OR NON()MASTER
S2    1630099   BIND????
S3    1986314   BUILDING()BLOCK? OR PROCESSOR? ? OR MEMOR????
S4    3247551   PARTITION? OR TERM()NOD??? OR SEGMENT? OR SECTOR? OR PORTI-
             ON? OR FRAGMENT?
S5     552706   PORT? ?
S6    7908200   FIRST OR SECOND? OR FORMER? OR LATTER?
S7      21155   S6(3N)S5
S8          0   S7 AND S1 AND S2 AND S3 AND S4
S9          3   S1 AND S2 AND S3
S10         3   RD (unique items)
S11      1498   S2 AND S3 AND S4
S12         2   S2 AND S3 AND S4 AND S7
S13         2   S12 NOT S10
S14        92   S2(10N)S3(10N)S4
S15        65   S2(6N)S3(6N)S4
S16        27   S2(3N)S3(3N)S4
S17        23   RD (unique items)
S18       252   S2 AND BUILDING(2N)BLOCK? AND S4
S19        13   S2(6N)BUILDING(N)BLOCK?(6N)S4
S20        10   RD (unique items)
S21         7   S20 NOT S10
S22       790   PARTITION?  AND BLOCK?  AND S5
S23       138   PARTITION?(10N)BLOCK?(10N)S5
S24         4   S23 AND IDENTIF?????
S25         3   S24 NOT S10
S26         3   RD S25 (unique items)
S27        11   S1 AND S3
S28         8   S27 NOT S10
S29         7   RD (unique items)
S30     98966   S3 AND S4
S31     14408   S3(3N)S4
S32       228   S4(3N)(BLOCK?(N)BUILD?)
S33       158   S4(2N)(BLOCK?(N)BUILD?)
S34         2   S33 AND S5
S35         1   S34 NOT S10
S36       155   S33 NOT S10
S37       126   RD (unique items)
S38        20   S37 AND PD<=20020109
S39    138299   S6(3N)(S5 OR S4)
S40        37   S39 AND S2 AND S3
S41        37   RD (unique items)
S42        36   S41 NOT S10
? show files
File   2:INSPEC 1969-2003/Oct W1
         (c) 2003 Institution of Electrical Engineers
File   6:NTIS 1964-2003/Oct W2
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2003/Oct W1
         (c) 2003 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Oct W1
         (c) 2003 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Sep
         (c) 2003 The HW Wilson Co.
File  94:JICST-EPlus 1985-2003/Oct W2
         (c)2003 Japan Science and Tech Corp(JST)
File 144:Pascal 1973-2003/Oct W1
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(c) 2003 INIST/CNRS
File 65:Inside Conferences 1993-2003/Oct W2
(c) 2003 BLDSC all rts. reserv.
File 35:Dissertation Abs Online 1861-2003/Sep
(c) 2003 ProQuest Info&Learning
File 347:JAPIO Oct 1976-2003/Jun(Updated 031006)
(c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200365
(c) 2003 Thomson Derwent
?

29/9/6 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02245259 **Image available**
CONTROL METHOD FOR **MASTERLESS** SERIAL BUS OCCUPATION

PUB. NO.: 62-162159 [JP 62162159 A]
PUBLISHED: July 18, 1987 (19870718)
INVENTOR(s): YAMAOKA HIROMASA
WAKITA AKIHIRO
SAITOU SUMIHISA
AMAHI YASUHIRO
SHIMOYAMA KAZUHIKO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI ENG CO LTD [323361] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-003434 [JP 863434]
FILED: January 13, 1986 (19860113)
INTL CLASS: [4] G06F-013/20; G06F-013/38
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- **Memory** Units)
JOURNAL: Section: P, Section No. 651, Vol. 11, No. 399, Pg. 79, December 26, 1987 (19871226)

ABSTRACT

PURPOSE: To attain the control of the occupation of a serial bus free from collision of data on a bus by obtaining an optimum transmission queuing time from a transmission PC number in a transmission data format, a transmission time interval set by a setting device, and the amount of transmission data in the transmission data format to set it in the counting devices of the respective PCs.

CONSTITUTION: An MPU 24 reads the self-PC number, the transmission interval, and the total PC number set in the setting device 27, and stores them in a **memory** 26. Then the MPU 24 sets the maximum queuing time in a counting device 25 and comes to a bus monitoring state in order to confirm that there is another PC on the serial bus currently being transmitted. In case there is no PC to be data-transmitted on the serial bus, the device 25 supplies to the MPU 24 a transmission timing after the lapsing of the maximum queuing time, and the MPU 24 executes the transmission. After ending the transmission, the MPU 24 gets again the maximum queuing time in the device 25, and executes the arithmetic and control operation. The above described operation is repeated thereafter.
?